IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Previously presented) A computer system having a plurality of resources, comprising:
a first processor coupled to a first bus;
a second processor coupled to a second bus; and
an instruction memory coupled to the first bus and the second bus and having a software direct memory access (DMA) engine stored therein, wherein
the software DMA engine is adapted to be executed by a processor of the first and second processors, the processor being coupled to the first bus and the second bus, and wherein
the software DMA engine is capable of transferring data directly between all of the plurality of resources, each of the plurality of resources being connected to at least one of the first bus and the second bus.

2. (Previously Presented) The system of Claim 1, wherein transferring data includes one or more of data processing, data filtering, data compacting and data reformatting.

3. (Original) The system of Claim 2, wherein the resources comprise one or more of static random access memory, dynamic random access memory and one or more hardware buffers that are capable of interfacing with one or more peripheral devices.

4. (Previously Presented) The system of Claim 3, wherein the one or more hardware buffers, in combination with the software DMA engine, permit the one or more peripherals to access the memory directly.

5. (Previously Presented) The system of Claim 3, wherein the software DMA engine comprises one or more instructions, the one or more instructions including a store multiple data instruction and a load multiple data instruction wherein, when executed by the processor:
the load multiple data instruction loads data from multiple locations in one of the hardware buffers into multiple locations in the internal registers in the processor, and
the store multiple data instruction transfers the data from multiple locations in the internal registers into multiple locations in a memory.

6. (Previously presented) A direct memory access (DMA) apparatus implemented in software on a computer system, the computer system having two or more processors and a memory coupled to each of the two or more processors, the DMA apparatus comprising:

a first instruction memory location in the computer system with a load multiple data instruction loaded therein; and

a second instruction memory location in the computer system with a store multiple data instruction loaded therein, wherein

the load multiple data instruction, when executed by a processor in the computer system, is capable of loading data from multiple locations in a resource into multiple locations in an internal register in the processor; and

the store multiple data instruction, when executed by the processor in the computer system, is capable of storing data from multiple locations in the internal register in the processor into multiple locations in a memory.

7. (Original) The apparatus of Claim 6, wherein the resources comprise one or more of static random access memory, dynamic random access memory and one or more hardware buffers that are capable of interfacing with one or more peripheral devices.

8. (Previously Presented) The apparatus of Claim 7, wherein the one or more hardware buffers, in combination with the DMA apparatus, permit the one or more peripherals to access the memory directly.

9. (Previously Presented) The apparatus of Claim 6, wherein the store multiple data instruction and the load multiple data instruction, when executed by the processor, each further include one or more of data processing, data filtering, data compacting and data reformatting.

10. (Canceled).